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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/731,134 | 12/10/2003 | Hsiao-Ying Yang | 0941-0871P | 4687 |

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

| EXAMINER | |
|---|---|
| KEBEDE, BROOK | |
| **ART UNIT** | **PAPER NUMBER** |
| 2823 | |

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/731,134 | YANG, HSIAO-YING | |
| | Examiner | Art Unit | |
| | Brook Kebede | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/10/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities:

The specification indicates the domestic priority in page 1, lines 4-5. However, it is not clear what is "CA" stands for. The examiner respectfully suggest to change "This application is a **CA** of patent application no. 10/405,613 to -- This application is a **continuation** of patent application no 10/405,613--. Appropriate correction is required.

The specification recites "the tunneling dielectric layer is oxide or oxynitride, such as $N_2O$, preferably formed by ..." in Page 6, lines 18-19. However, it is not clear what applicant is intended describe because, to the Examiner knowledge, there is no known dielectric layer such as $N_2O$ dielectric layer. If it is a typo, applicant is requested to make appropriate correction. Appropriate correction is required.

The specification recites "the gate interdielectric layer 230 is usually oxide/nitride/oxide (ONO), nitride/oxide (N/O), **MM'M''** $TiO_3$ formed by $TaO_2O_5$ (BST), wherein M comprises at least Ba, Sr, ..." in page 8, lines 8-11. However, it is not clear to the Examiner the chemical formula representation of **MM'M''** . Applicant is requested to make appropriate correction or explanation that describes **MM'M''**. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation " wherein the insulation layer is nitride " in lines 1-2. There is insufficient antecedent basis for "the insulation layer" in the claim. Therefore, the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**In light of the rejection 35 U.S.C. § 112 second Paragraph that set forth herein above, the following 35 U.S.C. 102 rejection for claim 6 is based on prior art which reads on the interpretation the claim language of the instant application as best as understood by the Examiner.**

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Hurley et al. (US/2002/0130357).

Re claim 1, Hurley et al. disclose a floating gate having improved coupling ratio, comprising: a semiconductor substrate (501); a tunneling dielectric layer (502) formed on the semiconductor substrate (501); a conductive layer (503), formed on the tunneling

dielectric layer (502) (see Figs. 5A-5F); and a plurality of conductive spacers (509), formed on the sidewalls of the conductive layer (503) (see Fig. 5G), and the tops of the conductive spacers level with the surface of the conductive layer, with the conductive spacers and the conductive layer forming the floating gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 2, as applied to claim 1above, Hurley et al. disclose all the claimed limitations including the limitation two neighboring shallow trench isolation structures (507), and the tunneling dielectric layer (502) (see Fig. 5C) located between the two shallow trench isolation structures (507) gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 3, as applied to claim 1above, Hurley et al. disclose all the claimed limitations including the limitation wherein the conductive layer is doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 4, as applied to claim 1above, Hurley et al. disclose all the claimed limitations including the limitation wherein the conductive spacers are doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 5, as applied to claim 1above, Hurley et al. disclose all the claimed limitations including the limitation wherein the tunneling dielectric layer is oxide or oxynitride (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 6, as applied to claim 1above, Hurley et al. disclose all the claimed limitations including the limitation wherein the insulation layer (504) (see Figs. 5A-5C) is nitride (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 7, Hurly et al. disclose a floating gate having improved coupling ratio, comprising: a semiconductor substrate (501); a tunneling dielectric layer (502) formed on the semiconductor substrate (501); a conductive layer (503), formed on the tunneling dielectric layer (502); a pair of shallow trench isolation (507) formed oppositely adjacent to the conductive layer (503), wherein the shallow trench isolation (507) is lower than the top surface of the conducting layer (503) (see Fig. 5D); and a plurality of conductive spacers (509), formed on the sidewalls of the conductive layer (503) and overlying the shallow trench isolation (507), and the tops of the conductive spacers (509) level with the surface of the conductive layer (503) (see Fig. 5G), with the conductive spacers and the conductive layer forming the floating gate (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 8, as applied to claim 7above, Hurley et al. disclose all the claimed limitations including the limitation wherein the conductive layer is doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 9, as applied to claim 7 above, Hurley et al. disclose all the claimed limitations including the limitation wherein the conductive spacers are doped polysilicon, doped amorphous silicon, undoped polysilicon, undoped amorphous silicon or polycide (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 10, as applied to claim 7 above, Hurley et al. disclose all the claimed limitations including the limitation wherein the tunneling dielectric layer is oxide or oxynitride (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

Re claim 11, as applied to claim 7 above, Hurley et al. disclose all the claimed limitations including the limitation wherein the shallow trench isolation is an oxide layer (see Figs. 1B; 5A-5G; Page 5, Paragraph [0060] through Paragraph [0067]).

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Ding et al (US/6,153,472), Lee (US/6,486,508), and Tuan et al. (US/6,562,681) also disclose similar inventive subject matter.

***Correspondence***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

Brook Kebede

BK
August 5, 2004